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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 10/646,997 | 08/22/2003 | Edward B. Harris | Downey 17-20/075903-200 | 1121 |

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| EXAMINER | |
|---|---|
| ROSE, KIESHA L | |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2822 | |

DATE MAILED: 06/14/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/646,997 | HARRIS ET AL. | |
| | Examiner | Art Unit | |
| | Kiesha L. Rose | 2822 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *07 March 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *21-27* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-20* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/22/03* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/23,1/30,3/18*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is in response to the election filed 7 March 2005.

### *Election/Restrictions*

Claims 21-27 are withdrawn from further consideration pursuant to 37 CFR 1.142(b), as being drawn to a nonelected method of making a semiconductor device, there being no allowable generic or linking claim. Applicant timely traversed the restriction (election) requirement in the reply filed on 7 March 2005. Applicants argue that the restriction was not correct that is erroneous since claims 1-20 are directed toward a device and claims 21-27 are directed toward a method of making the device and are considered two different inventions and are classified and searched in different classes and therefore require different searches.

Applicant's election with traverse of claims 1-20 in the reply filed on 7 March 2005 is acknowledged.

### *Drawings*

The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the conductive interconnect layer underlying the continuous conductor having an aperture formed therein must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. Each drawing sheet submitted after the filing date of an application must be labeled in the top margin as either "Replacement Sheet" or "New Sheet" pursuant to 37 CFR 1.121(d). If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

### *Claim Rejections - 35 USC § 102*

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1 and 4-8 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al. (U.S. Patent 6,153,489).

Park discloses an inductor (Fig. 2b) that contains a semiconductor substrate (10), a dielectric layer (14) overlying the substrate, a continuous conductor (16) disposed on the dielectric layer with first and second terminal ends (each individual layer 16), wherein the substrate defines an aperture (19) therein in at least a portion of a region underlying the continuous conductor

The continuous conductor is an inductor and comprises a spiral shape

A dielectric material (non-conductive semiconductor material) (filled in region 19 with silicon) disposed in the aperture

Where the size and geometric pattern of continuous conductor provide a desired inductance value

Claims 10-12 and 16 are rejected under 35 U.S.C. 102(b) as being anticipated by Park et al.

Park discloses an inductor (Fig. 2b) that contains a semiconductor substrate (10) with a plurality of active regions (substrate area around the trench (aperture)), a dielectric layer (12) overlying the substrate, one or more conductive interconnect layers (layer 14/17 with conductive layers in the dielectric), a continuous conductor (16) disposed on the dielectric layer in one of the conductive interconnect layers with first and second terminal ends (each individual layer 16), wherein the substrate defines an aperture (19) therein in at least a portion of a region underlying the continuous conductor, dielectric layer (14/17) disposed between conductive interconnect layers, dielectric material (non-conductive semiconductor material) (filled in region 19 with silicon) disposed in the aperture and conductive via (15) connecting one of the terminal

ends to an interconnect layer, the conductive interconnect layer (17) has apertures (spaces between the inductors) that are filled with non-conductive material .

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 2 and 3 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Beaussart et al. (U.S. Patent 6,429,504).

Park discloses all the limitations except for conductive vias formed in the dielectric between the upper surface of the dielectric and the active surface and which connect the first and second terminal ends. Whereas Beaussart discloses a spiral inductor (Fig. 5h) that contains a substrate (106) with an active region, a dielectric layer (108) overlying the substrate, aluminum conductive lines (104a-c) comprising an inductor with first and second terminal ends (each of the inductors a-c) and conductive vias (111-116) formed in the dielectric extending from the upper surface of the dielectric to the active surface. The plural conductive vias are formed in the dielectric layer to the active surface of the substrate from the conductive lines to supply an electrical connection. (Column 4, lines 21-26) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Park by incorporating plural conductive vias in the upper surface of the dielectric layer to

the active region from the conductive lines to supply an electrical connection as taught by Beaussart.

Claim 9 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Swanson (U.S. Patent 6,503,838).

Park discloses all the limitations except for the aperture extending from the upper surface to the lower surface. Whereas Swanson discloses an integrated circuit (Fig. 12) that contains a substrate (34) with an aperture (54) filled with a silicon layer with an inductor formed overlying the substrate. The substrate has an aperture to provide isolation for circuit components to minimize parasitic AC coupling. (Column 1, lines 12-16) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Park by incorporating an aperture in the substrate that extends from the upper surface to the lower surface to provide isolation for circuit components and to minimize parasitic AC coupling as taught by Swanson.

Claims 13-15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Beaussart.

Park discloses a plurality of active regions (substrate area around the trench (aperture)), a dielectric layer (12) overlying the substrate, one or more conductive interconnect layers (layer 14/17 with conductive layers in the dielectric), a continuous conductor (16) disposed on the dielectric layer in one of the conductive interconnect layers with first and second terminal ends (each individual layer 16), and conductive via (15) connecting one of the terminal ends to an interconnect layer. Park discloses all the

limitations except for conductive vias formed in the dielectric between the upper surface of the dielectric and the active surface and which connect the first and second terminal ends. Whereas Beaussart discloses a spiral inductor (Fig. 5h) that contains a substrate (106) with an active region, a dielectric layer (108) overlying the substrate, conductive lines (104a-c) comprising an inductor with first and second terminal ends (each of the inductors a-c) and conductive vias (111-116) formed in the dielectric extending from the upper surface of the dielectric to the active surface. The plural conductive vias are formed in the dielectric layer to the active surface of the substrate from the conductive lines to supply an electrical connection. (Column 4, lines 21-26) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Park by incorporating plural conductive vias in the upper surface of the dielectric layer to the active region from the conductive lines to supply an electrical connection as taught by Beaussart.

Claims 17-19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Park in view of Beaussart.

Park discloses a semiconductor substrate (10) having active regions (regions on the left and right of the aperture) formed therein, a dielectric layer (14) overlying the substrate, conductive lines (16) comprising an inductor formed overlying the upper surface and further comprising first and second terminal ends (each individual layer 16), a conductive via (15) and an aperture (19) in the substrate underlying at least a portion of the conductive lines and is filled with a dielectric material (non-conductive material). Park discloses all the limitations except for conductive vias formed in the dielectric

between the upper surface of the dielectric and the active surface and which connect the first and second terminal ends. Whereas Beaussart discloses a spiral inductor (Fig. 5h) that contains a substrate (106) with an active region, a dielectric layer (108) overlying the substrate, conductive lines (104a-c) comprising an inductor with first and second terminal ends (each of the inductors a-c) and conductive vias (111-116) formed in the dielectric extending from the upper surface of the dielectric to the active surface. The plural conductive vias are formed in the dielectric layer to the active surface of the substrate from the conductive lines to supply an electrical connection. (Column 4, lines 21-26) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the device of Park by incorporating plural conductive vias in the upper surface of the dielectric layer to the active region from the conductive lines to supply an electrical connection as taught by Beaussart.

Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Park, Beaussart and Swanson.

Park and Beaussart disclose all the limitations except for the aperture extending from the upper to lower surface of the substrate. Whereas Swanson discloses an integrated circuit (Fig. 12) that contains a substrate (34) with an aperture (54) filled with a dielectric material that extends from the upper surface to the lower surface of the substrate. The aperture is formed from the upper surface to lower surface to expose to porous silicon from the backside. (Column 5, lines 52-55) Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to modify the devices of Park and Beaussart by incorporating the aperture to extend from

the upper surface to lower surface of the substrate to expose the porous silicon from the backside as taught by Swanson.

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kiesha L. Rose whose telephone number is 571-272-1844. The examiner can normally be reached on M-F 8:30-6:00 off 2nd Mondays.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amir Zarabian can be reached on 571-272-1852. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

KR
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